Department of Electronics & Communication Engineering

Laboratory Details

Sl No.	Name of the Laboratory	No. of Students per setup (Batch size)	Name of the Important equipment	Experiments conducted
1.	BASIC ELECTRONICS LAB	Maximum 30	• Cathod Ray Oscilloscope • Function Generator • D.C. Power Supply • A.C. Power Supply • Digital Multimeter • AC different Power Supply • DC power Suppply with digital display	1. Familiarization with passive and active electronic components such as Resistors, Inductors, Capacitors, Diodes, Transistors (BJT) and electronic equipment like DC power supplies, millimeters etc. 2. Familiarization with measuring and testing equipment like CRO, Signal generators etc. 3. Study of I-V characteristics of Junction diodes. 4. Study of I-V characteristics of Zener diodes. 5. Study of Half and Full wave rectifiers with Regulation and Ripple factors. 6. Study of I-V characteristics of BJTs. 7. Study of I-V characteristics of Field Effect Transistors. 8. Determination of input-offset voltage, input bias current and Slew rate of OPAMPs.
2	ANALOG ELECTRONICS LAB	Maximum 30	• Digital Storage Oscilloscope • Cathod Ray Oscilloscope • Function generator • Analog-Digital Trainer Kit • D.C. Power Supply • A.C. Power Supply	1. Design of RC coupled amplifier in CE mode & study of it's frequency response using BJT. 2. Design of RC Phase shift oscillator using BJT and measurement of its output frequency. 3. Design of Wien bridge oscillator using BJT and measurement of its output frequency. 4. Design of class A & class B push-pull power amplifiers and measurement of its power conversion efficiency. 5. Design of single stage voltage amplifier & study of it's frequency response using

				JFET. 6. Design of differential amplifier & study of it's frequency response using BJT. 7. Design of practical Integrator using OPAMP (IC-741) and study of its frequency response. 8. Design of practical Differentiator using OPAMP (IC-741) and study of its frequency response.
3	DIGITAL ELECTRONIC S LAB	Maximum 30	• Cathod Ray Oscilloscope • Digital Trainer Kit • I.C. Tester	1. Realization of basic gates using Universal logic gates. 2. Design the circuit of Grey to Binary and vice versa. 3. Design a circuit for BCD to 7-segment display. 4. Construction of simple Encoder & Decoder circuits using logic gates. 5. Construction of simple Multiplexer & De Multiplexer circuits using logic gates. 6. Design of Half Adder & Full Adder Circuit using Logic Gates. 7. Design Half Subtractor & Full Subtractor Circuit using Logic Gates. 8. Realization of RS, D, JK and T flip-flops using logic gates.
4	ANTENNA & PROPAGATI ON LAB	Maximum 30	• Microwave Test bench setup • Basic Antenna Training Setup • Advance Antenna Training System • Transmission Line Trainer &Analyser • Power Meter • Power Sensor • Spectrum Analyzer • Antenna Measurement System • Cathod Ray Oscilloscope • Vector Network Analyzer	1. Familiarization of basic elements of Transmission Line. 2. Plotting of Standing Wave Pattern along a transmission line when the line is open-circuited, short-circuited and terminated by a resistive load at the load end. 3. Unknown load Impedance of a terminated transmission line using shift in minima technique. 4. Study of application of Smith chart by using characteristic of transmission line. Familiarization of basics of Antennas. 5. Radiation Pattern of dipole antenna and Mono-pole with ground plane. 6. Radiation Pattern of a

				folded-dipole antenna. 7. Radiation pattern of a Log-Periodic Antenna. 8. Study Single stub impedance matching technique.
5	MICROWAVE ENGINEERING LAB	Maximum 30	• Microwave Test bench setup • Digital Storage Oscilloscope	1. Familiarization of basic elements of Transmission Line. 2. Plotting of Standing Wave Pattern along a transmission line when the line is open-circuited, short-circuited and terminated by a resistive load at the load end. 3. Unknown load Impedance of a terminated transmission line using shift in minima technique. 4. Study of application of Smith chart by using characteristic of transmission line. 5. Study Single stub impedance matching technique. Familiarization of basics of Antennas. 7. Radiation Pattern of dipole antenna and Mono-pole with ground plane. 8. Radiation Pattern of a folded-dipole antenna.
6	ANALOG & DIGITAL COMMUNICATION LAB	Maximum 30	• Amplitude Modulation Transmitter Kit • Amplitude Demodulator kit • Selectivity-Sensisitivity fidelity of a Super-hetrodyne receiver kit. • Frequency Modulation trainer Kit • Frequency Demodulation Kit • Frequency Modulation Kit • Frequency Demodulation Kit • VCO Trainer kit ,ETB-90 PLL Tranier Kit • TDM pulse Amplitude Modulation & Demodulation Trainer • Data Conditioning and reconditioning Kit • Pulse Width Modulation & Demodulation Kit • Pulse Amplitude /pulse Width /Pulse Position	1. Measurement of output power with varying modulation index an AM signal (for both DSB- & SSB). 2. Measurement of the demodulated output with varying modulation index of an AM signal (for both DSB-SC & SSB). 3. Measurement of power of different frequency components of a frequency modulated signal & the measurement of the bandwidth. 4. Design a PLL using VCO & to measure the lock frequency. 5. Study of pulse amplitude modulation (PAM) and demodulation. 6. Study of PCM and demodulation.

			Modulation & Demodulation Kit • Pulse code Modulation Demodulation kit • Pulse code Modulation kit • Pulse code Demodulation kit • Delta/Sigma Delta & Adaptive Delta Modulation & Demodulation Kit • QPSK & DQPSK De Modulation Kit • Distortion METER • Digital Storage Oscilloscope • Cathod Ray Oscilloscope • Function Generator,	7. Study of delta modulator and demodulator 8. Study of ASK modulator and demodulator
7	DIGITAL SIGNAL PROCESSINC LAB	Maximum 30	i)DSP Kit(5416) , ii)DSP Kit(6713) , iii)Matlab 2013 5 users license version software, iv)University Program for Micro Tutor Lab Kit, v)Computer Set-Dell(i5 processor, 8GB RAM, 1TB HDD), vi)Computer Set-Dell(i3 processor, 4GB RAM, 500 GB HDD-Micro CPU) ,vii)Computer Set-Accer(i3 processor,2 GB RAM,500 GB HDD), viii)Computer Set-LENOVO(3.3GHz CPU,2GB RAM, 300GB HDD ,ix)Computer Set-HP(2.93GHz CPU,896MB RAM,97.6GB HDD, x)Computer Set-Dell(i3 processor, 4GB RAM, 1TB HDD)	1. Convolution of two sequences using graphical methods and using commands-verification of the properties of convolution. 2. Systems (Causal and Non_causal, Time-Invarient and Time-varient etc.) verification using MATLAB. 3. Z-transform of various sequences – verification of the properties of Z-transform. 4. DFT using twiddle factors. 5. DFTs / IDFTs using matrix multiplication and also using commands. 6. Circular convolution of two sequences using graphical methods and using commands, differentiation between linear and circular convolutions. 7. Verifications of the different algorithms associated with filtering of long data sequences and Overlap –add and Overlap-save methods. 8. Butterworth filter design with different set of parameters.
8	VLSI Lab	Maximum 30	i)UPS ,ii)6U RACK (Steel Valrack) with VR FAN For RACK ,iii)T SPICE Pro-5 users license software (TANNER EDA Tool), iv)Mentor Graphics IC Nanometer Design Bundle software, v)Arduino UNO, vi) Raspberry pi 3B, vii)Computer Set-Dell(i5 processor, 8GB RAM, 1TB HDD), viii)Computer Set-	1. SPICE simulation of CMOS inverter to plot voltage transfer characteristics (VTC) for different values of ratio for VDD=1 V and nano dimensional channel length a) Measurement of critical voltages VIL , VIH, VOL , VOH from VTC . b) Calculation of noise margin

			Dell(i3 processor, 4GB RAM, 500 GB HDD-Micro CPU) ,ix)Computer Set-Accer(i3 processor,2 GB RAM,500 GB HDD), x)Computer Set-LENOVO(3.3GHz CPU,2GB RAM, 300GB HDD ,xi)Computer Set-HP(2.93GHz CPU,896MB RAM,97.6GB HDD, xii)Computer Set-Dell(i3 processor, 4GB RAM, 1TB HDD)	from critical voltages. 2. Functional verification, gate delay and average power consumption analysis of CMOS inverter circuit for VDD $\leq$ 1.2 V and with the nano dimensional channel length of MOS transistor through SPICE simulation. 3. Design and testing of functionality of the following gate and combinational circuit with the help of SPICE tools at schematic level. a) CMOS AND / NAND, OR/NOR, XOR/XNOR gate b) CMOS full adder circuit 4. Layout design and functional verification of CMOS inverter, CMOS NAND, CMOS NOR gate using layout design tools of SPICE based on design rules. 5. Design and examination of functionality of the sequential circuits - CMOS SR latch, clocked SR latch & D flip-flop at schematic level using SPICE tools. 6. Design and simulation with the help of VHDL applying suitable modelling style (structural, behavioural, dataflow, mixed) for the following combinational circuits a) Logic gates b) Full adder using half adder c) 4:1 MUX using 2:1 MUX 7. Design using VHDL for the following Sequential circuits a) S-R Flip-Flop b) 8-bit synchronous counter c) 8 Bit bi-directional register with tri-stated input output 8. Familiarity with FPGA based system design and realization of 4:1 Mux using FPGA.
9	EMBEDDED SYSTEM AND IOT LAB	Maximum 30	• COMPUTER SET 15 Desktop Dell Vostro 3471 SFF.9th Generation Intel Core-i5 9400 (9MB	**1. Programming with ARM processor/ Raspberry Pi/Arduino:** i) Introduction to Raspberry Pi and Arduino programming ii) LED interfacing with

			Cache, up to 4.1GHz) 1x4 GB DDR4, 2666MHz, scalable up to 32GB/1TB 7.2 K RPM SATA Hard Drive /No optical drive Ubuntu Linux 18.04/18.5" Monitor. with inbuilt Wireless 1707 Card (802.11BGN Bluetooth 4.0, 2.4 GH 2.MICRO TUTOR KIT SET.	Raspberry Pi/Arduino iii) Proximity sensor interfacing with Raspberry Pi/Arduino iv) Ultrasonic sensor interfacing with Raspberry Pi/Arduino v) Servo motor interfacing with Raspberry Pi/Arduino vi) Seven segment display interfacing with Raspberry Pi/Arduino **2. Programming with Atmega8/16/328P processor:** i) LED interfacing with Atmega8/16/328P ii) Proximity sensor interfacing with Atmega8/16/328P iii) Ultrasonic sensor interfacing with Atmega8/16/328P

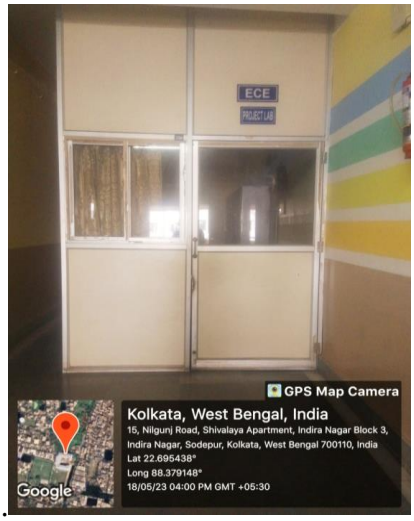
Project Laboratory

The Department is having it's two Project and research laboratories which are functioning under the Departmental R and D Cell. These laboratories are established with the partial support of funding from Govt. agencies like UGC, DST and AICTE etc. in addition to the seed funding from the university. Main objective of these labs are providing the required research facilities in various emerging areas of Electronics & communication Engineering. The details of projects undergone in these laboratories along with the major equipment available and the resulting publications are listed below-

1. Project Laboratory I-

Utilization 90 % through student projects –

Under graduate students utilize this lab mainly to design the prototypes of their hardware or software projects



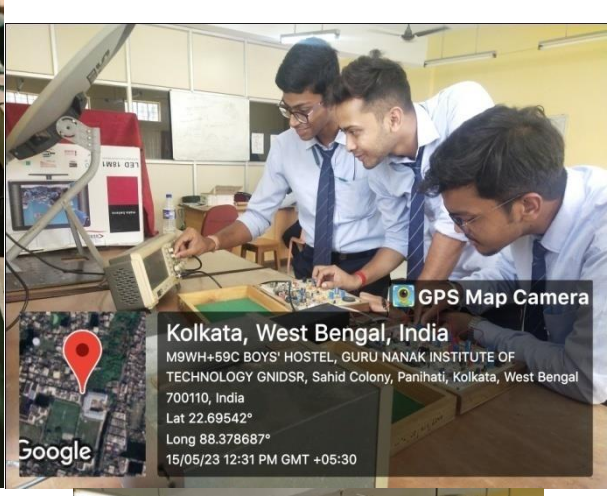
Project Laboratory I

Project laboratory II :

This laboratory is mainly used for both student and faculty research and development activity.

Figure 6.4.b Project Laboratory II


Kolkata, West Bengal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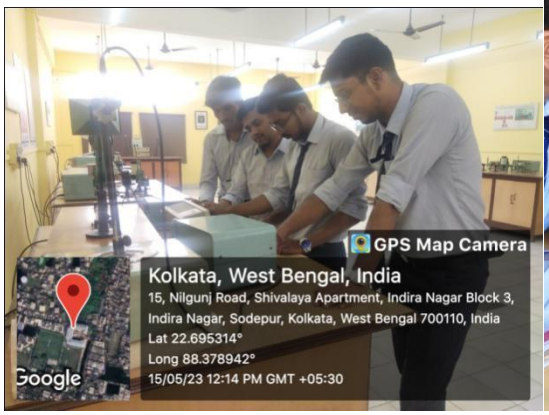
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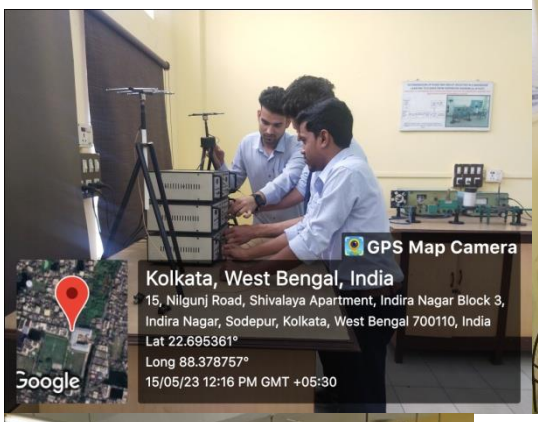
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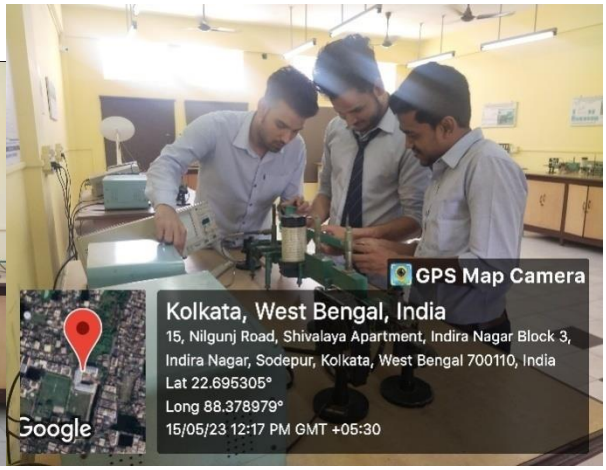
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